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EXAMINER	
DAVENPORT, MON CHERI S	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,832	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	MON CHERI S. DAVENPORT	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 2-16, and 21-22** rejected under 35 U.S.C. 103(a) as being unpatentable over Choe et al. (US Patent 7,254,111) in view of Hass et al. (US Patent Application Publication 2003/0120876).

Regarding **Claim 21** Choe et al. disclose a communication control device comprising (see figure 2, section 200, parallel router, see also col. 4, lines 57-60, massively parallel router):

a plurality of processors which perform predetermined parallel processing cooperatively(see figure 2, see col. 4, lines 57-60, massively parallel router);

a plurality of processor interfaces having one or more cell distributors and one or more selectors, in which each of said processors is connected to one of said cell distributors and one of said selectors (see figure 2, see also col. 5 lines 32-41, the routing node comprises an input-output processor, which are connected as shown in figure 2); and

an internal communication path which connects said cell distributor said selectors, said plurality of processors, a first external communication path, and a second external communication path(see figure 2, see col. 5, lines 56-59, each router node is linked by switch fabrics 250A and 250B)

wherein said cell distributors receive communication cells from said internal communication path and transfer the received communication cells to the corresponding processor when the destination of the received communication cells are the corresponding processor (see col. 5, lines the routing nodes (processors) are linked together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);

wherein said cell distributors are coupled to receive communication cells from said internal communication path and output said communication cells onto said internal communication path when the destination of said received communication cells is not to the corresponding processor ((see col. 5, lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);

wherein the communication control device processes said communication cells received from the first external communication path and transmits the communication cells to the second external communication path (see figure 2, see col. 5, lines 4—45, each one of the IOP(input-output processors) buffer incoming data from the external router 290 and network 295).

Choe et al. fails to specifically point out wherein said selectors receive communication cells from said corresponding processor and output the said communication cells onto said internal communication path when possessing a transmission rights ;

wherein said transmission rights are received and possessed by is granted to only one selector at a time and said selectors abandon said transmission rights by outputting

said transmission rights when said selectors end the selector the outputting of the communication cells received from the corresponding processor as claimed.

However Hass et al. teaches wherein said selectors receive communication cells from said corresponding processor and output the said communication cells onto said internal communication path when possessing a transmission rights (see figure 1, ring based multiprocessing system, see [0060], lines 1-6, multiprocessors exchange data with each other in a data ring, which reads on communicating when processing a transmission right);

Hass et al teaches wherein said transmission rights are received and possessed by is granted to only one selector at a time and said selectors abandon said transmission rights by outputting said transmission rights when said selectors end the selector the outputting of the communication cells received from the corresponding processor (see [0060] lines 1-5, the multiprocessors implement the data ring through a set of point-to-point connection, which reads on transmission rights to only one processing unit at a time).

Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to combine Choe et al. invention with Hass et al. invention because Hass et al. invention is a multiprocessor which efficiently manages processing resources and memory transfers (see Hass et al. [0028], lines 1-6).

Regarding **claim 22** Choe et al. discloses a communication control device comprising (see figure 2, section 200, parallel router, see also col. 4, lines 57-60, massively parallel router):

at least a first and a second processor which perform predetermined parallel processing cooperatively (see Figure 2, section IOP (input-output processors) see col. 4, lines 57-60, massively parallel router) ;

at least a first cell distributor connected to at least said first processor and a second cell distributor connected to at least said second processor(see figure 2, section PMD(physical medium devices, see col. 5, lines 52-58, each PMD card frames incomming packets, which are connected by the switch fabric to a second processor);

at least a first selector connected to at least said first cell distributor and said first processor and a second selector connected to at least said second cell distributor and second processor (see figure 2, section PMD(physical medium devices, see col. 5, lines 52-58, each PMD card frames incomming packets, which are connected by the switch fabric to a second processor);;

at least a first external communication path and a second external communication path(see figure 2, see col. 5, lines 4—45, each one of the IOP(input-output processors) buffer incoming data from the external router 290 and network 295); and

an internal communication path which connects at least said first and second cell distributors, said first and second selectors, said first and second processors, and said first and second external communication paths ((see col. 5, lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);:

wherein said first cell distributor receives communication cells via said internal communication path and transfers said received communication cells to said first processor when the destination of said received cell is said first processor ((see col. 5,

lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);

wherein said second cell distributor receives communication cells via said internal communication path and transfers said received communication cells to said second processor when the destination of said received cell is said second processor ((see col. 5, lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);

wherein said first cell distributor receives communication cells via said internal communication path and transfers said received communication cells to said first selector when the destination of said received cell is not said first processor ((see col. 5, lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);:

wherein said second cell distributor receives communication cells via said internal communication path and transfers said received communication cells to said second selector when the destination of said received cell is not said second processor ((see col. 5, lines the routing nodes (processors) are linked (coupled) together by the switch fabric which allows the transfer of the received communication cells as shown in figure 2);

wherein said communication control device processes said communication cells received from said first external communication path and transmits said communication cells to said second external communication path(see figure 2, see col. 5, lines 4—45, each one of the IOP(input-output processors) buffer incoming data from the external router 290 and network 295).

Choe et al fails to specifically point out wherein said first selector receives said communication cells from said first processor and outputs said communication cells onto said internal communication path when possessing a transmission rights: wherein said second selector receives said communication cells from said second processor and outputs said communication cells onto said internal communication path when possessing said transmission rights: wherein said first selector possesses said transmission rights when said first selector receives a token cell and loses said transmission rights when said first selector outputs said token cell after said communication cells have been output: wherein said second selector possesses said transmission rights when said second selector receives a token cell and loses said transmission rights when said second selector outputs said token cell after said communication cells have been output: wherein said token cell is possessed by one selector at a time as claimed.

However Hass et al. teaches wherein said first selector receives said communication cells from said first processor and outputs said communication cells onto said internal communication path when possessing a transmission rights(see figure 1, ring based multiprocessing system, see [0060], lines 1-6, multiprocessors exchange data with each other in a data ring, which reads on communicating when processing a transmission right);

wherein said second selector receives said communication cells from said second processor and outputs said communication cells onto said internal communication path when possessing said transmission rights(see figure 1, ring based multiprocessing system, see [0060], lines 1-6, multiprocessors exchange data with each other in a data ring, which reads on communicating when processing a transmission right);

wherein said first selector possesses said transmission rights when said first selector receives a token cell and loses said transmission rights when said first selector outputs said token cell after said communication cells have been output (see [0060] lines 1-5, the multiprocessors implement the data ring through a set of point-to-point connection, which reads on transmission rights to only one processing unit at a time):

wherein said second selector possesses said transmission rights when said second selector receives a token cell and loses said transmission rights when said second selector outputs said token cell after said communication cells have been output (see [0060] lines 1-5, the multiprocessors implement the data ring through a set of point-to-point connection, which reads on transmission rights to only one processing unit at a time):

wherein said token cell is possessed by one selector at a time(see [0060] lines 1-5, the multiprocessors implement the data ring through a set of point-to-point connection, which reads on transmission rights to only one processing unit at a time);

Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to combine Choe et al. invention with Hass et al. invention because Hass et al. invention is a multiprocessor which efficiently manages processing resources and memory transfers (see Hass et al. [0028], lines 1-6).

Regarding **Claim 2** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein said internal communication path connects said cell distributors and said selectors in a ring as claimed.

However Hass et al. teaches wherein said internal communication path connects said cell distributors and said selectors in a ring (see [0060], lines 1-2, processors exchange data with each other in a data ring).

Regarding **Claim 3** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 2*). In addition the communication control device includes:

Choe et al. fails to specifically point out comprising a token cell generator for generating a token cell used to grant said transmission rights to one of said selectors, and outputting said token cell onto said internal communication path as claimed.

However Hass et al. teaches comprising a token cell generator for generating a token cell used to grant said transmission rights to one of said selectors, and outputting said token cell onto said internal communication path(see [0063], lines 1-14, the global snoop controller responds, and the snoop request instructs each cluster to transfer ownership of the requested memory indicating it does not posses the requested location, which reads on a transmission rights in which ownership is transferred i.e. when the token cell is used to grant transmission rights).

Regarding **Claim 4** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 3*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein said token cell generator is said selector as claimed.

However Hass et al. teaches wherein said token cell generator is said selector (see figure 1, section Global snoop controller, see [0057], lines 1-6, global snoop controller manages data sharing between the clusters).

Regarding **Claim 5** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 3*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein said token cell generator is provided in said cell distributor as claimed.

However Hass et al. teaches wherein said token cell generator is provided in said cell distributor(see figure 1, section Global snoop controller, see [0057], lines 1-6, the global snoop controller issues snoop instructions to clusters on a snoop ring).

*(*Regarding **Claim 6** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 3*). In addition the communication control device includes:

wherein said selector outputs a communication cell received from a connected processor onto said internal communication path when said token cell is possessed thereby(see col. 5, lines 56-58, each router node is connected via internal communication path . switch fabrics 250A, and 250B as shown in figure 2).

Regarding **Claim 7** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 3*). In addition the communication control device includes:

wherein said selector outputs said token cell onto said internal communication path after outputting all of the communication cells received from a connected processor (see col. 5, lines 45-48, each IOP forwards packets to the outbound IOP)

Regarding **Claim 8** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). In addition the communication control device includes:

wherein said internal communication path comprises a common bus connected to said cell distributors and said selectors (see col. 5, lines 56-58, each router node is connected via internal communication path switch fabrics 250A, and 250B as shown in figure 2).

Regarding **Claim 9** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 8*). In addition the communication control device includes:

Choe et al. fail to specifically point out comprising a transmission rights manager for granting said transmission rights to one of said selectors as claimed.

Hass et al. teaches comprising a transmission rights manager for granting said transmission rights to one of said selectors (see figure 1, section Global snoop controller, see [0057], lines 1-6, global snoop controller manages data sharing, reads on transmission rights, between the clusters).

Regarding **Claim 10** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 9*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein, when a request for transmission rights is received from one of said selectors, said transmission rights manager grants transmission rights to said selector after another selector has lost transmission rights as claimed.

However Hass et al. teaches wherein, when a request for transmission rights is received from one of said selectors, said transmission rights manager grants transmission rights to said selector after another selector has lost transmission rights (see [0060], lines 1-6, the transmission rights are exchanges with each other in a logical data ring, through a set of point to point connections).

Regarding **Claim 11** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 9*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein said transmission rights manager is provided in each of said processor interfaces as claimed.

However Hass et al. teaches wherein said transmission rights manager is provided in each of said processor interfaces (see figure 1, global snoop controller which is provided and connected to each of the processor interfaces).

Regarding **Claim 12** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 11*). In addition the communication control device includes:

Choe et al. fails to specifically point out wherein, when a request for transmission rights is received from one of said selectors, said transmission rights manager grants said

transmission right to the selector after receiving information indicating the assignment or loss of said transmission rights from another transmission rights manager as claimed.

However Hass et al. teaches wherein, when a request for transmission rights is received from one of said selectors, said transmission rights manager grants said transmission right to the selector after receiving information indicating the assignment or loss of said transmission rights from another transmission rights manager (see [0060], lines 1-6, the transmission rights are exchanges with each other in a logical data ring, through a set of point to point connections, which transmission right are given from point to point).

Regarding **Claim 13** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). In addition the communication control device includes:

wherein said processor interface comprises a buffer unit for temporarily storing communication cells transferred to a connected processor from said cell distributor(see col. 5, lines 45-52,each IOP maintains (memory) internal; routing tables, and processing the incoming packet from the PMD).

Regarding **Claims 14 and 16** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 13*). In addition the communication control device includes:

wherein said buffer unit comprises(see figure 2, PMD, physical medium device)

a buffer for temporarily storing communication cells (see figure 2, PMD, physical medium device)

a cell writer for writing communication cells received from said cell distributor to said buffer (see figure 2, PMD and IOP (input-output processor))and

a cell reader for reading the communication cells stored in said buffer and transmitting the communication cells to said processor (see figure 2, section IOP (input-output processor, reads and processing incoming packets)

Regarding **Claim 15** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). In addition the communication control device includes:

wherein said processor interface comprises a buffer unit for temporarily storing communication cells transmitted from said processor to said selector (see figure 2, section 220, routing node, PMB and IOP, stores and processes commuication cells transmitted).

3. Claims **17-18, and 20** rejected under 35 U.S.C. 103(a) as being unpatentable over Choe et al. in view of Hass et al. in view further in view of Ikeda et al. (US Patent Number 5,896,501).

Regarding **Claim 17** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). However Choe et al. in view of Hass et al. fails to specifically disclose that the processor interface comprises a format converter for converting the format of communication cells received from another of said processor interfaces via said internal communication path as claimed.

Ikeda et al. discloses wherein said processor interface comprises a format converter for converting the format of communication cells received from another of said

processor interfaces via said internal communication path (see Ikeda et al., figure 1, address translator, see col 5, lines 15-19, the transfer control section writes or reads data to or from the storage according to a real address translated by the inherent address translator section, or the common address translator section, as a result data is transferred between one processor and another).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide Choe et al. in view of Hass et al. with Ikeda et al. because Ikeda et al.'s invention provides a method for transferring data in a shorter time within a multiprocessor system (see Ikeda et al. col. 2, lines 6-10).

Regarding **Claim 18** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 21*). However Choe et al. in view of Hass et al. fails to specifically disclose wherein said processor interface comprises a format converter for converting the format of communication cells to be transmitted to another of said processor interfaces via said internal communication path as claimed.

Ikeda et al. discloses processor interface comprises a format converter for converting the format of communication cells to be transmitted to another of said processor interfaces via said internal communication path (see Ikeda et al., figure 1, address translator, see col 5, lines 15-19, the transfer control section writes or reads data to or from the storage according to a real address translated by the inherent address translator section, or the common address translator section, as a result data is transferred between one processor and another).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide Choe et al. in view of Hass et al. with Ikeda et al. because Ikeda et al.'s invention provides a method for transferring data in a shorter time within a multiprocessor system (see Ikeda et al. col. 2, lines 6-10).

Regarding **Claim 20** Choe et al. in view of Hass et al. discloses everything as applied above (*see claim 19*). However Choe et al. in view of Hass et al. fails to specifically disclose the communication control device comprising a format converter for converting the format of communication cells received onto said internal communication path from said externals and the format of communication cells to be transmitted to said externals from said internal communication path as claimed.

Ikeda et al. discloses the communication control device comprising a format converter for converting the format of communication cells received onto said internal communication path from said externals (see Ikeda et al., figure 1, address translator, see col 5, lines 15-19, the transfer control section writes or reads data to or from the storage according to a real address translated by the inherent address translator section, or the common address translator section, as a result data is transferred between one processor and another) and the format of communication cells to be transmitted to said externals from said internal communication path (see figure 3, see col ,2, lines 28-32, a transfer control section write or reads data to or from a storage according to the real address translated by the inherent address translator section or by the common address translator section, thus data is transferred between the one processor and another processor).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide Choe et al. in view of Hass et al. with Ikeda et al. because Ikeda et al.'s invention provides a method for transferring data in a shorter time within a multiprocessor system (see Ikeda et al. col. 2, lines 6-10).

Response to Arguments

4. Applicant's arguments with respect to claims 2-18 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MON CHERI S. DAVENPORT whose telephone number is (571)270-1803. The examiner can normally be reached on Monday - Friday 8:00 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Seema S. Rao/
Supervisory Patent Examiner, Art Unit 2416

/Mon Cheri S Davenport/
Examiner, Art Unit 2416
October 21, 2008